82437FX System Controller (TSC) and 82438FX Data Path Unit (TDP)

Timing Specification

Datasheet Addendum

Product Features

- Supports the Pentium® Processor at iCOMP® Index 1110\133 MHz, iCOMP Index 1000\120 MHz, iCOMP Index 815\100 MHz, iCOMP Index 735\90 MHz and the iCOMP Index 610\75 MHz
- Integrated Second Level Cache Controller
  - —Direct Mapped Organization
  - —Write-Back Cache Policy
  - —Cacheless, 256-Kbyte, and 512-Kbyte
  - —Standard Burst and Pipelined Burst SRAMs
  - —Cache Hit Read/Write Cycle Timings at 3-1-1-1 with Burst or Pipelined Burst SRAMs
  - —Back-to-Back Read Cycles at 3-1-1-1-1-1-1-1 with Burst or Pipelined Burst SRAMs
  - —Integrated Tag/Valid Status Bits for Cost Savings and Performance
  - —Supports 5 V SRAMs for Tag Address
- Integrated DRAM Controller
  - —64-Bit Data Path to Memory
  - —4 Mbytes to 128 Mbytes Main Memory
  - —EDO/Hyper Page Mode DRAM (x-2-2-2 Reads) or Standard Page Mode DRAMs
  - —4 Qword Deep Buffer for 3-1-1-1 Posted Write Cycles
  - —5 RAS Lines
  - —Symmetrical and Asymmetrical DRAMs
  - —3 V or 5 V DRAMs
- EDO DRAM Support
  - —Highest Performance with Burst or Pipelined Burst SRAMs
  - —Superior Cacheless Designs
- Fully Synchronous 25/30/33 MHz PCI Bus Interface
  - —100 Mbyte/s Instant Access Enables Native Signal Processing on Pentium Processors
  - —Synchronized CPU-to-PCI Interface for High Performance Graphics
  - —PCI Bus Arbiter: PIIX and Four PCI Bus Masters Supported
  - —CPU-to-PCI Memory Write Posting with 4 Dword Deep Buffers
  - —Converts Back-to-Back Sequential CPU to PCI Memory Writes to PCI Burst Writes
  - —PCI-to-DRAM Posting of 12 Dwords
  - —PCI-to-DRAM up to 120 Mbytes/s Bandwidth Utilizing Snoop Ahead Feature
- NAND Tree for Board-Level ATE Testing
- 208-Pin QFP for the 82437FX System Controller (TSC); 100 Pin QFP for Each 82438FX Data Path (TDP)

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheets published for the Intel 430FX PCIset. Please refer to the standard 430FX datasheet (order number 290518) for TSC and TDP product information and specifications not found in this document.

Order Number: 297463-001
May 1998

Datasheet Addendum

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1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Maximum Rating
Case Temperature under Bias	0° C to +85° C
Storage Temperature	-55° C to +150° C
Voltage on Any Pin with Respect to Ground	-0.3 to VDD + 0.3 V
Supply Voltage with Respect to Vss	-0.3 to +6.5 V
Maximum Power Dissipation	2.0 W

Warning: *Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.*

1.2 Thermal Characteristics

The 82437FX TSC and 82438FX TDP are designed for operation at case temperatures between 0° C and 85° C. The thermal resistances of the TSC and TDP packages are given in Table 1 and Table 2, respectively.

Table 1. 82437FX (TSC) Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/W)	31	24.5
θ_{jc} (°C/W)	8.6	

Table 2. 82438FX (TDP) Package Thermal Resistance

Parameter	Air Flow Meters/Second (Linear Feet per Minute)	
	0 (0)	1.0 (196.9)
θ_{ja} (°C/W)	89	67
θ_{jc} (°C/W)	29	

1.3 DC Characteristics

Table 3. 82437FX DC Characteristics

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Notes 1,6; VDD3=3.135V
V_{IH1}	Input High Voltage	2.2	VDD3 + 0.3	V	Notes 1,7; VDD3=3.6V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2; VDD=4.75V
V_{IH2}	Input High Voltage	2.2	VDD + 0.3	V	Note 2; VDD=5.25V
V_{OL1}	Output Low Voltage		0.4	V	Note 3
V_{OH1}	Output High Voltage	2.4		V	Note 3
I_{OL1}	Output Low Current		1	mA	
I_{OH1}	Output High Current	-1		mA	
I_{OL2}	Output Low Current		3	mA	Note 4
I_{OH2}	Output High Current	-2		mA	Note 4
I_{OL3}	Output Low Current		6	mA	Note 5
I_{OH3}	Output High Current	-2		mA	Note 5
I_{IH1}	Input Leakage Current		±10	µA	0V<Vin<VDD
I_{IH2}	Input Leakage Current		±300	µA	Note 8; 0V<Vin<VDD
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	FC = 1 MHz
I_{CC}	V_{CC} Supply Current		345 40	mA mA	5V Supply 3V Supply

NOTES:

1. V_{IL1} and V_{IH1} apply to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#, SMIACT#, PLINK[15:0]
2. V_{IL2} and V_{IH2} apply to the following signals: TIO[7:0], RST#, AD[31:0], C/BE[3:0]#, PLOCK#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PAR, REQ[3:0]#, PCMD[1:0], PCLKIN, HCLKIN
3. V_{OL1} and V_{OH1} apply to the following signals: TIO[7:0], TWE#, CADV#/CAA4, CADS#/CAA3, COE#, CWE[7:0]#, A[31:3], KEN#, AHOLD, BRDY#, NA#, BOFF#, EADS#, PLINK[15:0], PCMD[1:0], MSTB#, MADV#, HOE#, POE#, MOE#, MAA[1:0], MAB[1:0], MA[11:2], CAS[7:0]#, AD[31:0], CCS#/CAB4, CAB3, RAS[4:0]#, GNT[3:0]#, PHLDA, AD[31:0], C/BE[3:0]#, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, PLOCK#
4. I_{ol2} and I_{oH2} apply to the following signals: AD[31:0], C/BE[3:0]#, PAR
5. I_{ol3} and I_{oH3} apply to the following signals: FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#, GNT[3:0]#
6. For transient voltages, V_{IL1} min is Vss - 1.4V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.
7. For transient voltages, V_{IH1} max is VDD3 + 1.7V. This applies to the following signals: A[31:3], BE[7:0]#, D/C#, W/R#, M/IO#, HLOCK#, ADS#, HITM#, CACHE#.
8. I_{IH2} applies to the following signals: TIO[7:0], REQ[3:0]#, PHOLD. These signals have internal pullup resistors.

Table 4. 82438FX DC Characteristics

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage	-0.3	0.8	V	Notes 1,8; VDD3=3.135V
V_{IH1}	Input High Voltage	2.2	VDD3 + 0.3	V	Notes 1,9; VDD3=3.6V
V_{IL2}	Input Low Voltage	-0.3	0.8	V	Note 2; VDD=3.135V/ 4.75V
V_{IH2}	Input High Voltage	2.2	VDD + 0.3	V	Note 2; VDD=3.6V/5.25V
V_{OL1}	Output Low Voltage		0.4	V	Note 3
V_{OH1}	Output High Voltage	VDD - 0.7		V	Note 3
V_{OL2}	Output Low Voltage		0.4	V	Note 4
V_{OH2}	Output High Voltage	VDD3 - 0.7		V	Note 4
I_{OL1}	Output Low Current		1	mA	Note 5
I_{OH1}	Output High Current	-1		mA	Note 5
I_{OL2}	Output Low Current		4	mA	Note 6
I_{OH2}	Output High Current	-4		mA	Note 6
I_{IL1}	Input Leakage Current		±10	µA	0<Vin<VDD
I_{IL2}	Input Leakage Current		±700	µA	Note 7; 0<Vin<VDD
C_{IN}	Input Capacitance		12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance		12	pF	F_C = 1 MHz
$C_{I/O}$	I/O Capacitance		12	pF	F_C = 1 MHz
I_{CC}	V_{CC} Supply Current		250 60	mA mA	5V Supply 3V Supply

NOTES:

1. V_{IL1} and V_{IH1} apply to the following signals: HD[31:0], MOE#, POE#, HOE#, MADV#, MSTB#, PCMD[1:0], PLINK[7:0]
2. V_{IL2} and V_{IH2} apply to the following signals: MD[31:0]. VDD is dependent on VDD3/5 strapping.
3. V_{OL1} and V_{OH1} apply to the following signals: MD[31:0]. VDD is dependent on VDD3/5 strapping.
4. V_{OL2} and V_{OH2} apply to the following signals: HD[31:0] and PLINK[7:0].
5. I_{OL1} and I_{OH1} apply to PLINK[7:0].
6. I_{OL2} and I_{OH2} apply to MD[31:0] and HD[31:0].
7. I_{IL2} applies to MD[31:0] and HD[31:0]. These signals have internal pull-down resistors.
8. For transient voltages, V_{IL1} minimum is Vss - 1.4V. This applies to the following signals: HD[31:0] and MD[31:0].
9. For transient voltages, V_{IH1} maximum is VDD3 + 1.7V. This applies to the following signals: HD[31:0] and MD[31:0].

1.4 82437FX AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified.

Table 5. Host Clock Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t1	HCLKIN Period	15.0	20.0	16.7	20.0	1	
	HCLKIN Period Stability		±250		±250		ps
t3	HCLKIN High Time	5.5		5.5		1	
t4	HCLKIN Low Time	5.5		5.5		1	
t5	HCLKIN Rise Time		1.2		1.2	1	
t6	HCLKIN Fall Time		1.2		1.2	1	
	HCLKIN Rising Edge to PCLKIN Rising Edge Skew	1	6	1	6		HCLKIN must lead PCLKIN

Table 6. CPU Interface Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t7	ADS# Setup Time to HCLKIN Rising	5.0		5.5		4	
t7a	W/R# Setup Time to HCLKIN Rising	6.0		6.5		4	
t8	BE[7:0]# Setup Time to HCLKIN Rising	5.0		5.5		4	
t10	HITM# Setup Time to HCLKIN Rising	6.0		6.5		4	
t11	CACHE# Setup Time to HCLKIN Rising	5.0		5.5		4	
t11a	M/IO# Setup Time to HCLKIN Rising	6.0		6.5		4	
t12	D/C# Setup Time to HCLKIN Rising	5.0		5.5		4	
t13	HLOCK#, SMIACT# Setup Time to HCLKIN Rising	5.0		5.5		4	
t14	ADS#, HITM#, W/R#, M/IO#, D/C#, BE[7:0], HLOCK#, CACHE#, SMIACT# Hold Time from HCLKIN Rising	1.0		1.0		4	
t15	A[31:3] Setup Time to HCLKIN Rising	3.0		3.0		4	
t16	A[31:3] Hold Time from HCLKIN Rising	1.0		1.0		4	
t17	A[31:3] Output Enable From HCLKIN Rising	0.0	13.0	0.0	13.5	8	
t18	A[31:3] Valid Delay from HCLKIN Rising	2.0	13.0	2.0	13.5	3	0 pF
t19	A[31:3] Float Delay from HCLKIN Rising	0.0	13.0	0.0	13.5	5	
t21	BRDY# Valid Delay from HCLKIN Rising	1.5	8.0	1.5	8.5	3	0 pF
t22	NA# Valid Delay from HCLKIN Rising	1.5	8.0	1.5	8.5	3	0 pF
t23	AHOLD Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t24	BOFF# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t25	EADS# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t26	KEN#/INV Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF

Table 7. Second Level Cache Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
Asynchronous and Burst SRAMs							
t27	COE# Valid Delay from HCLKIN Rising	2.0	9.0	2.0	9.5	3	0 pF
t28	TIO [7:0] Valid Delay from HCLKIN Rising	2.0	9.0	2.0	9.5	3	0 pF
t28a	TIO[7:0] Flow through Delay to BRDY#, NA#, CWE[7:0]#	2.0	10.0	2.0	10.5	6	
t29	TIO[7:0] Setup time to HCLKIN Rising	2.0		2.5		4	
t30	TIO[7:0] Hold time from HCLKIN Rising	2.0		2.0		4	
t31	TWE# Valid Delay from HCLKIN Rising	2.0	9.0	2.0	9.5	3	0 pF
Asynchronous SRAMs Only							
t32	CWE[7:0]# Valid Delay from HCLKIN Rising	3.0	13.0	3.0	13.5	3	0 pF
t33	CAA[4:3], CAB[4:3]# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
Burst SRAMs Only							
t34	CWE[7:0]# Valid Delay from HCLKIN Rising	2.0	9.5	2.0	10.0	3	0 pF
t35	CCS# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t36	CADS# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t37	CADV# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF

Table 8. DRAM Interface Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t42	RAS[4:0]# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t42a	MOE# Valid Delay From HCLKIN Rising	1.5	7.0	1.5	7.5	3	
t44	CAS[7:0]# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t46	MA[11:2] Valid Delay from HCLKIN Rising on first clock after RAS# assertion	2.0	9.0	2.0	9.5	3	0 pF, 13 Ohms
t47a	MAA[1:0], MAB[1:0] Valid Delay from HCLKIN Rising	2.0	8.0	2.0	8.5	3	0 pF
t47b	MA[11:2], MAx[1:0] Flow Through Delay for a Read Cycle	2.0	12.5	2.0	13.0	6	Leadoff, 0 pF
t47c	MA[11:2], MAx[1:0] Valid Delay from HCLKIN Rising for a Refresh Cycle	2.0	12.5	2.0	13.0	3	Leadoff, 0 pF
t47d	MA[11:2], MAx[1:0] Valid Delay from HCLKIN Rising for PCI-to-DRAM Read Cycle	2.0	16.0	2.0	16.5	3	Leadoff, 0 pF
t47e	MA[11:2], MAx[1:0] Valid Delay from HCLKIN Rising for a Write Cycle	2.0	18.0	2.0	18.5	3	Leadoff, 0 pF

Table 9. PCI Clock Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t49	PCLKIN High Time	12.0		12.0		1	
t50	PCLKIN Low Time	12.0		12.0		1	
t51	PCLKIN Rise Time		3.0		3.0	1	
t52	PCLKIN Fall Time		3.0		3.0	1	

Table 10. PCI Interface Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t53	AD[31:0] Valid Delay from PCLKIN Rising	2	11	2	11	3	Min: 0 pF Max: 50 pF
t54	AD[31:0] Setup Time to PCLKIN Rising	7		7		4	
t55	AD[31:0] Hold Time from PCLKIN	0		0		4	
t56	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Valid Delay from PCLKIN Rising	2	11	2	11	3	Min: 0 pF Max: 50 pF
t57	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Output Enable Delay from PCLKIN Rising	2		2		8	
t58	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Float Delay from PCLKIN Rising	2	28	2	28	5	
t59	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Setup Time to PCLKIN Rising	7		7		4	
t60	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, LOCK#, PAR, DEVSEL# Hold Time from PCLKIN Rising	0		0		4	
t61	PHLDA# Valid Delay from PCLKIN Rising	2	9.0	2	9.0	3	Min: 0 pF Max: 50 pF
t65	PHLD# Setup Time to PCLKIN Rising	12		12		4	
t66	PHLD# Hold Time from PCLKIN Rising	0		0		4	
t67	GNT[3:0] # Valid Delay from PCLKIN Rising	2	9.0	2	9.0	3	Min: 0 pF Max: 50 pF
t68	REQ[3:0]# Setup Time to PCLKIN Rising	12		12		4	
t69	REQ[3:0]# Hold Time from PCLKIN Rising	0		0		4	
t70	RST# Low Pulse Width	1 ms		1 ms		7	

Table 11. TDP Interface Timing; 60 MHz and 66 MHz (82437FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t71	HOE# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t72	MOE# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t73	POE# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t74	MSTB# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t75	MADV# Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t76	PCMD [1:0] Valid Delay from HCLKIN Rising	1.5	7.0	1.5	7.5	3	0 pF
t77	PLINK[15:0] Valid Delay from HCLKIN Rising	2.0	7.5	2.0	8.0	3	0 pF
t78	PLINK[15:0] Setup Time to PCLKIN Rising	3.0		3.5		4	
t79	PLINK[15:0] Hold Time from PCLKIN Rising	2.5		2.5		4	

1.5 82438FX AC Characteristics

Table 12. Host Clock Timing; 60 MHz and 66 MHz (82438FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t80	HCLK Period	15.2	20.0	16.7	20.0	1	
t81	HCLK High Time	5.5		5.5		1	
t82	HCLK Low Time	5.5		5.5		1	
t83	HCLK Rise Time		1.5		1.5	1	
t84	HCLK Fall Time		1.5		1.5	1	
t85	HCLK Period Stability		±250		±250		ps

Table 13. Command Signal Timing; 60 MHz and 66 MHz (82438FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t86	MOE# Setup Time to HCLKIN Rising	3.0		3.5		4	
t87	MOE# Hold Time to HCLKIN Rising	1.5		1.5		4	
t88	HOE# Setup Time to HCLKIN Rising	3.0		3.5		4	
t89	HOE# Hold Time to HCLKIN Rising	1.5		1.5		4	
t90	POE# Setup Time to PCLKIN Rising	3.0		3.5		4	
t91	POE# Hold Time to PCLKIN Rising	1.5		1.5		4	
t92	MADV# Setup Time to HCLKIN Rising	5.0		5.5		4	
t93	MADV# Hold Time from HCLKIN Rising	1.5		1.5		4	
t94	MSTB# Setup Time to HCLKIN Rising	3.0		3.5		4	
t95	MSTB# Hold TIme to HCLKIN Rising	1.5		1.5		4	
t96	PCMD[1:0] Setup Time to HCLKIN Rising	4.0		4.5		4	
t97	PCMD[1:0] Hold Time to HCLKIN Rising	1.5		1.5		4	
t98	PLINK[7:0] Setup Time to HCLKIN Rising	3.0		3.5		4	
t99	PLINK[7:0] Hold Time to HCLKIN Rising	2.0		2.0		4	
t100	PLINK [7:0] Output Valid Delay to HCLKIN Rising	2.0	9.0	2.0	9.5	3	0 pF

Table 14. Address/data Timing: 60 MHz and 66 MHz (82438FX)

Functional Operating Range (VDD = 5 V ±5%, VDD3 = 3.135 V to 3.6 V; T_{CASE} = 0° C to +85° C)

Symbol	Parameter	66 MHz		60 MHz		Fig.	Notes
		Min	Max	Min	Max		
t101	D[31:0] Valid Delay from HCLKIN Rising	1.4	7.5	1.4	8.0	3	0 pF
t102	D[31:0] Setup Time to HCLKIN Rising Host Bus	3.0		3.5		4	
t103	D[31:0] Hold Time from HCLK Rising Host Bus	1.5		1.5		4	
t104	MD[31:0] Valid Delay from HCLKIN Rising	1.7	11.0	1.7	11.5	3	0 pF
t105	MD[31:0] Setup Time to MADV# Falling	3.0		3.5		4	
t106	MD[31:0] Hold Time from MADV# Falling	1.0		1.0		4	

1.6 82437FX/82438FX Timing Diagrams

Figure 1. Clock Timing

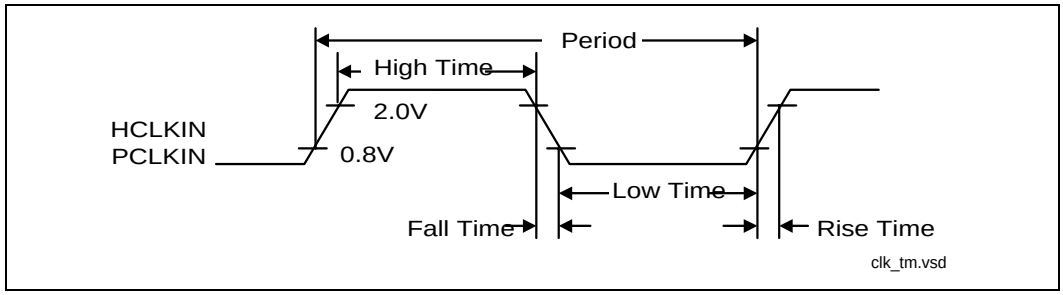


Figure 2. Propagation Delay

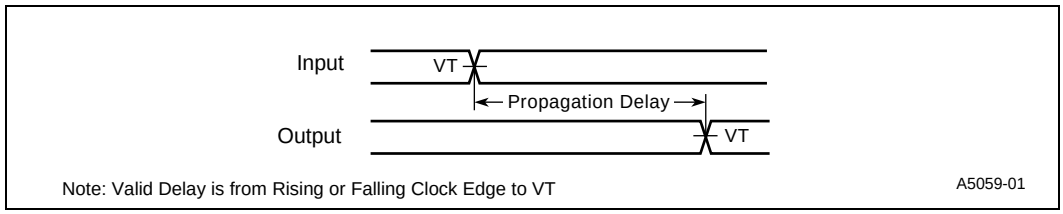


Figure 3. Valid Delay From Rising Clock Edge

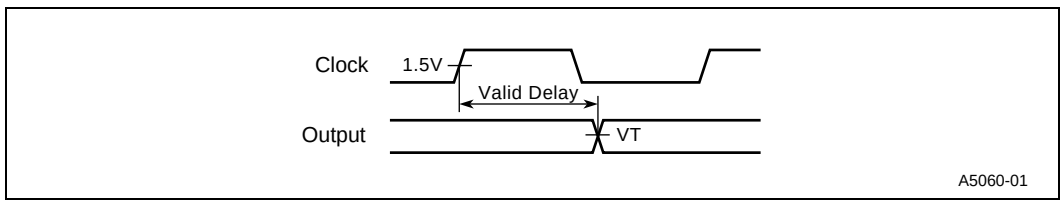


Figure 4. Setup and Hold Times

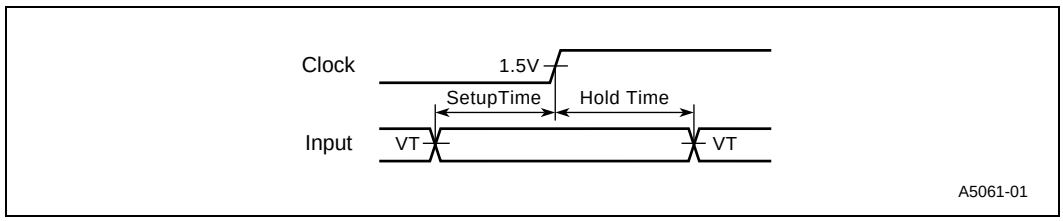


Figure 5. Float Delay

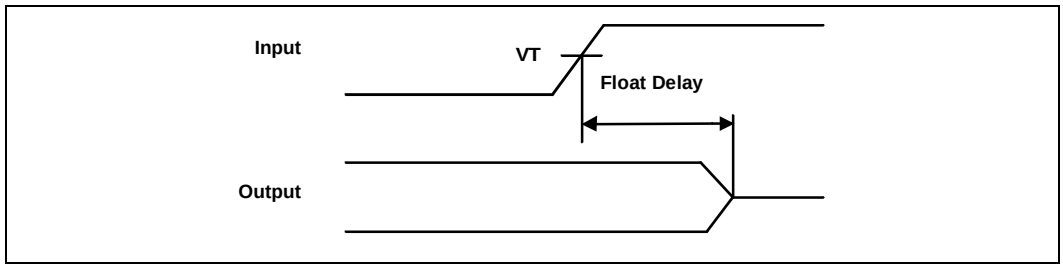
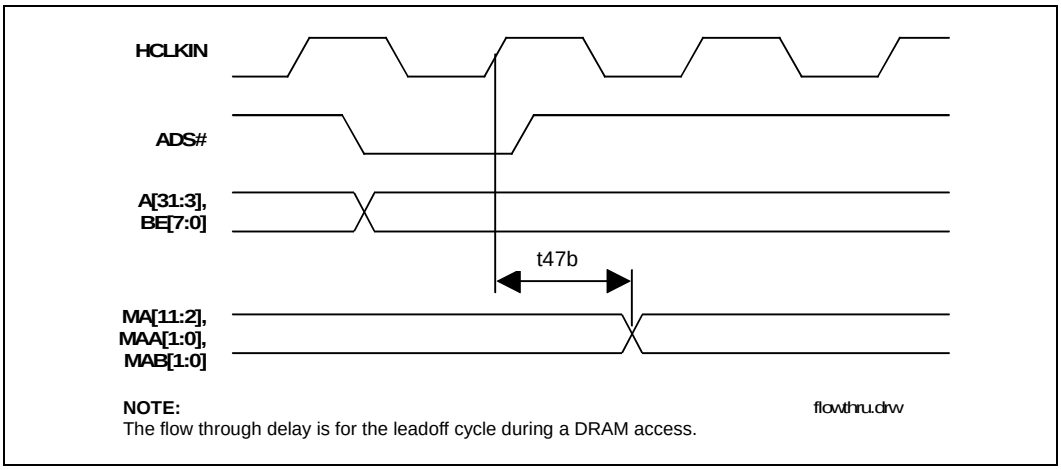


Figure 6. Flow Through Delay



NOTE:
The flow through delay is for the leadoff cycle during a DRAM access.

Figure 7. Pulse Width

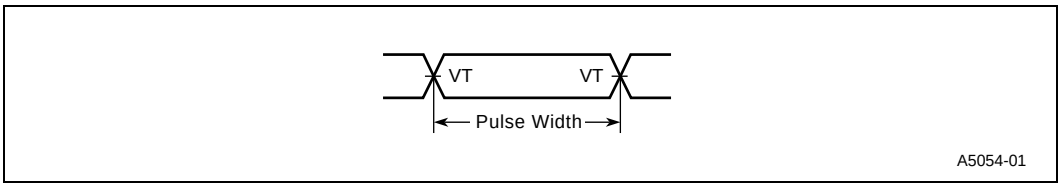
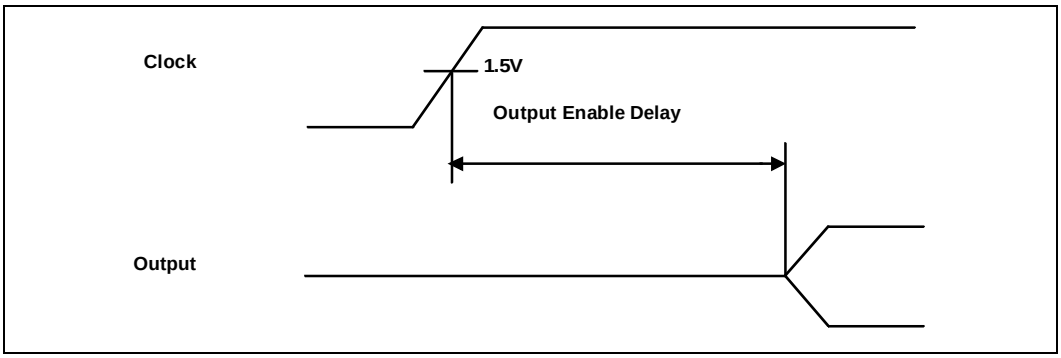


Figure 8. Output Enable Delay



2.0 Timing Relationship Diagrams

2.1 Cache Timing Relationships

Figure 9. Burst Read (L1 Line Fill), Standard SRAM

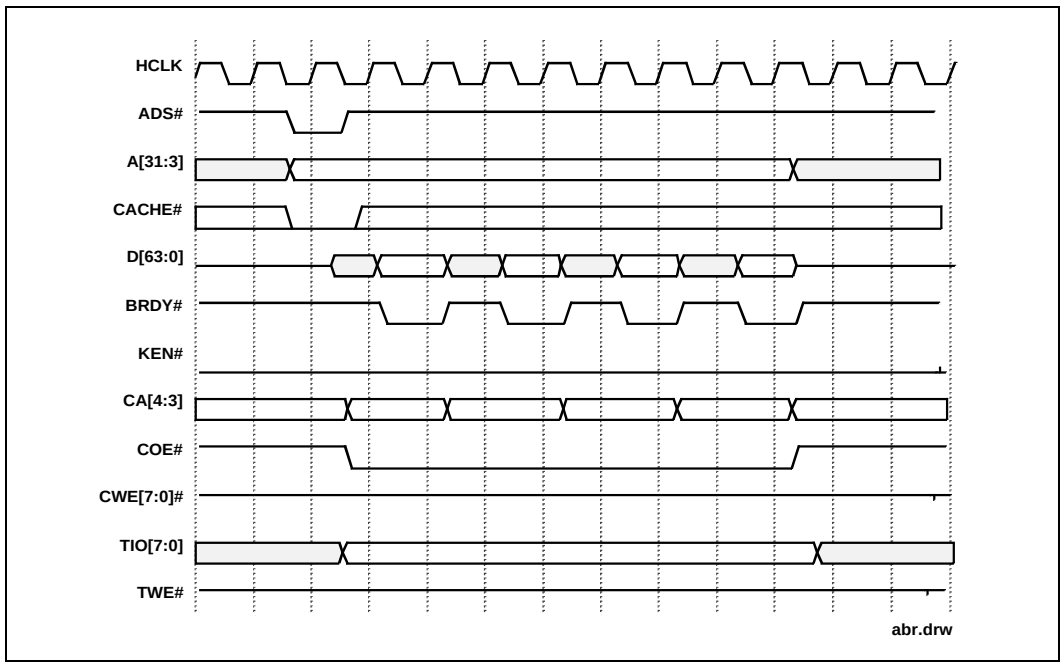


Figure 10. Burst Write (L1 Cache Write-Back), Standard SRAM

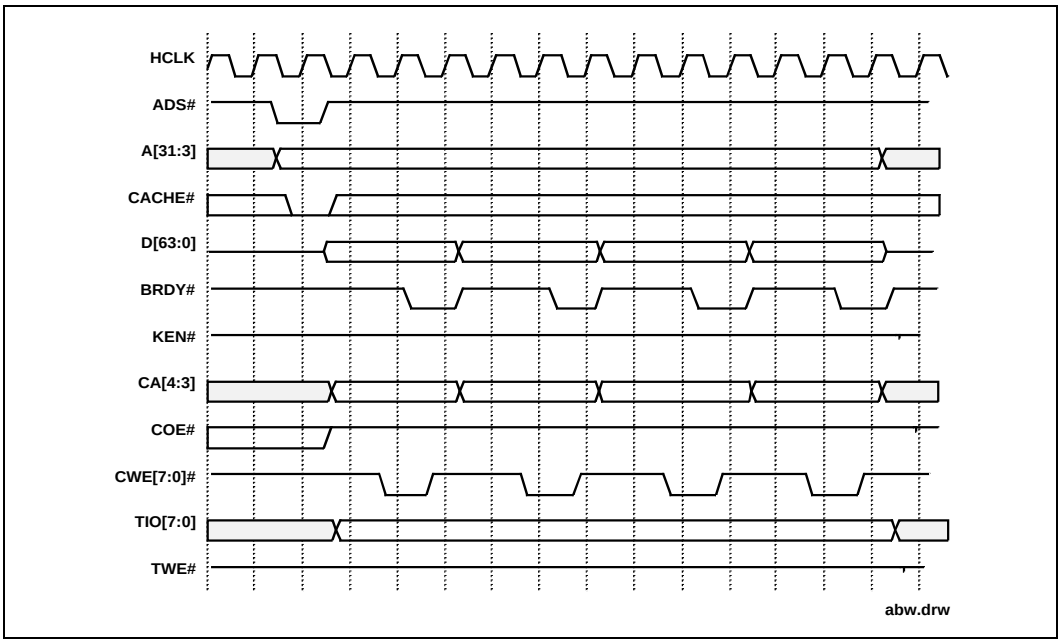


Figure 11. Back to Back Burst Reads (L1 Cache Line Fills), Standard SRAM

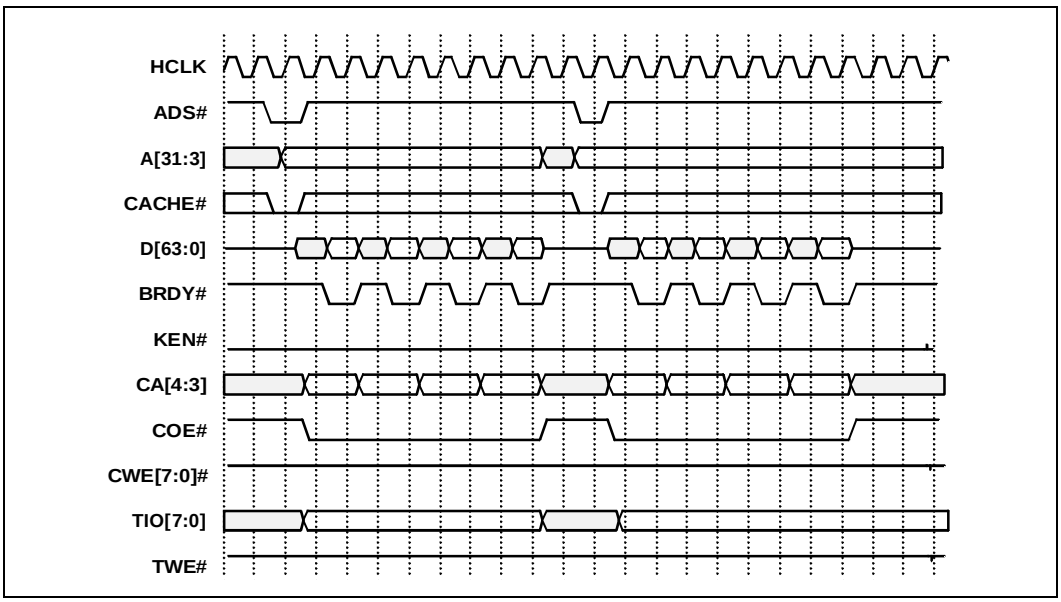


Figure 12. Second Level Cache Read Miss, Write-Back, Line Fill with Pipelined Burst SRAM

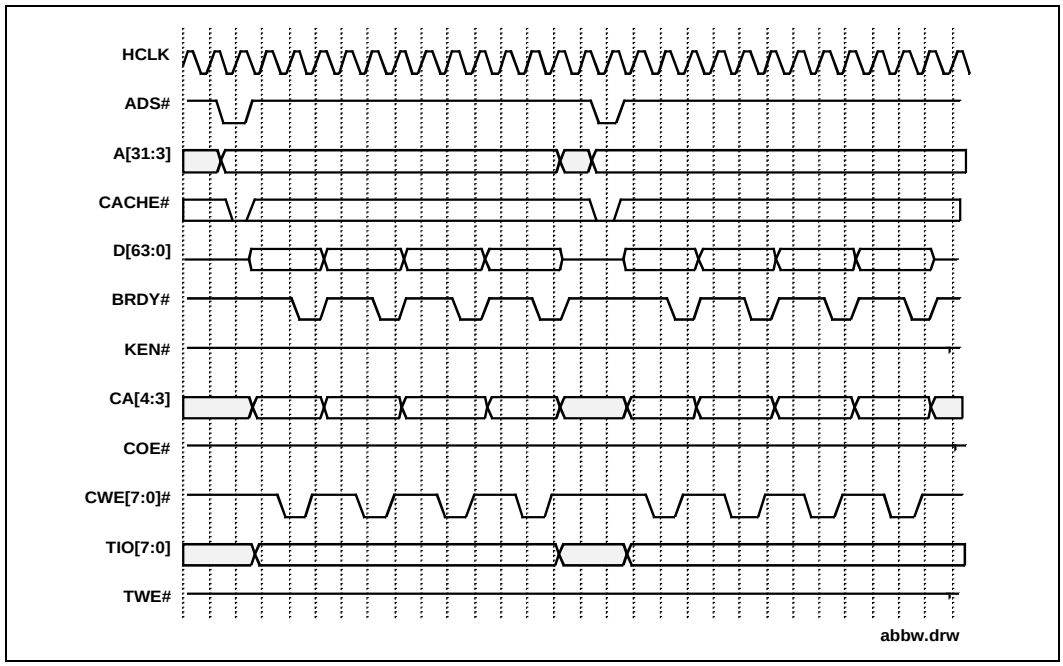


Figure 13. Read Miss, L2 Cache Write-Back, Line Fill, Standard SRAM

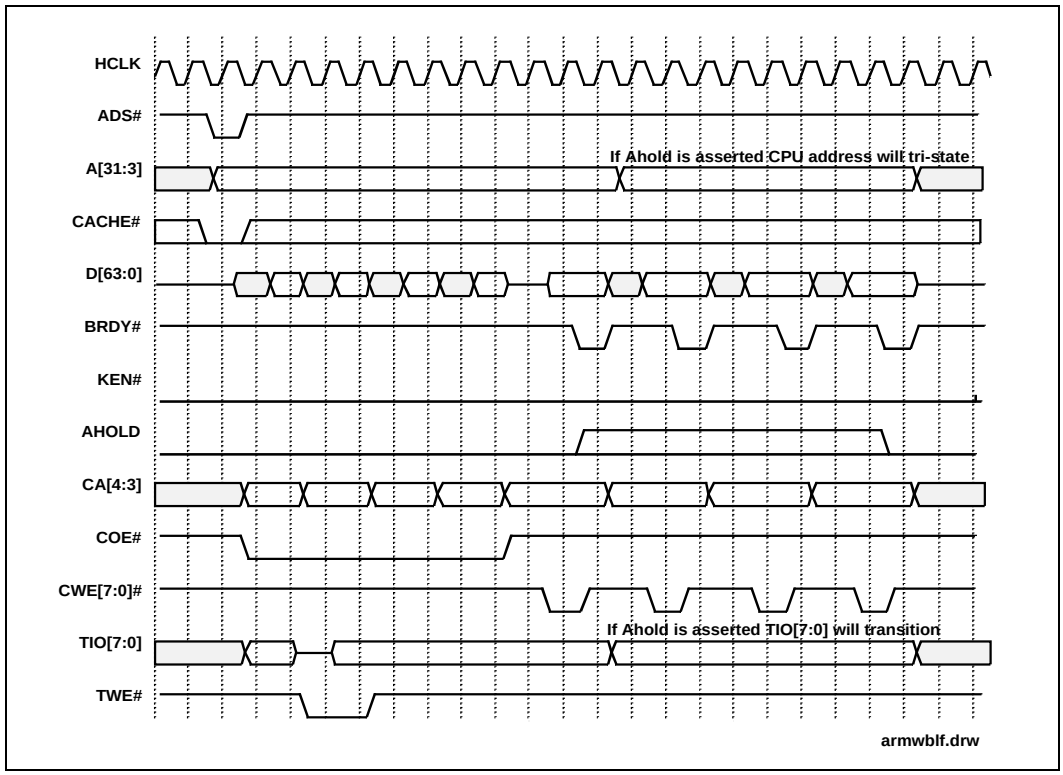


Figure 14. Burst Read, Pipelined Burst SRAM

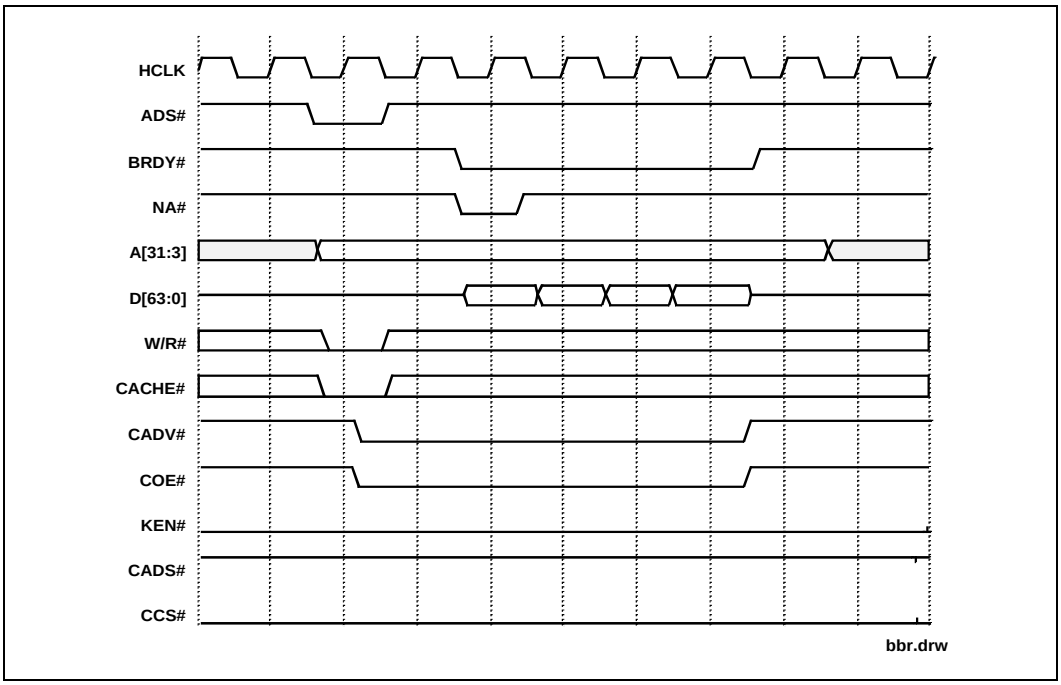


Figure 15. Back-to-Back Reads (L1 Cache Line Fills), Pipelined Burst SRAM

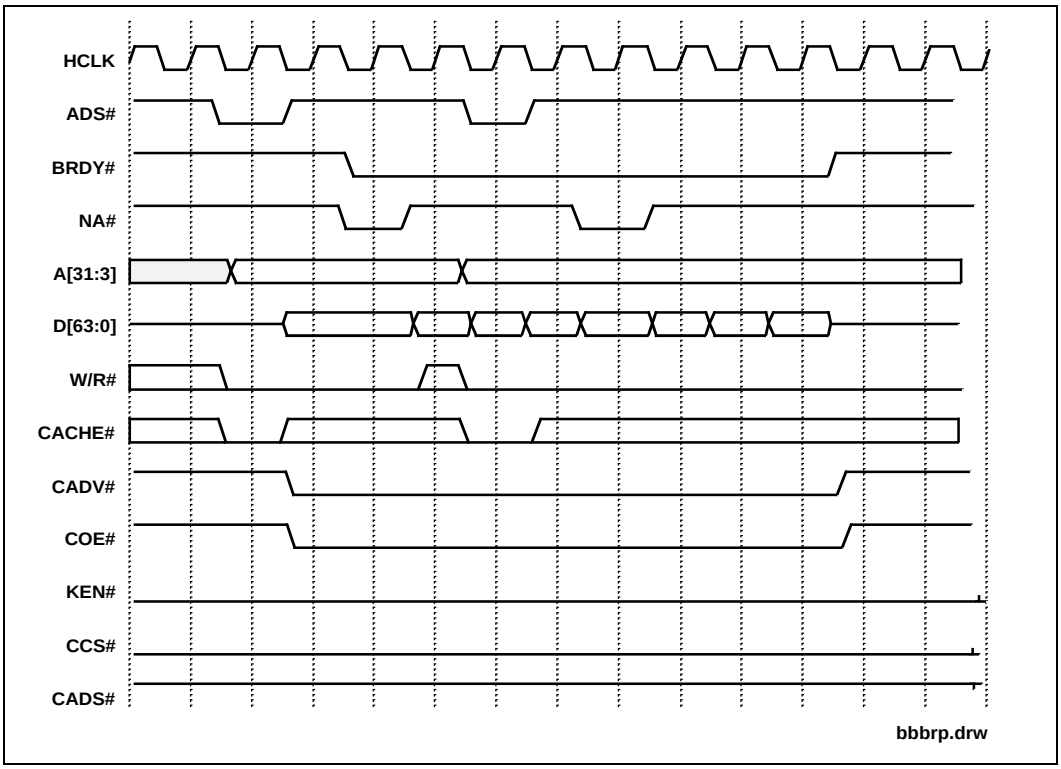


Figure 16. Back-to-Back Writes (L1 Cache Line Fills), Pipelined Burst SRAM

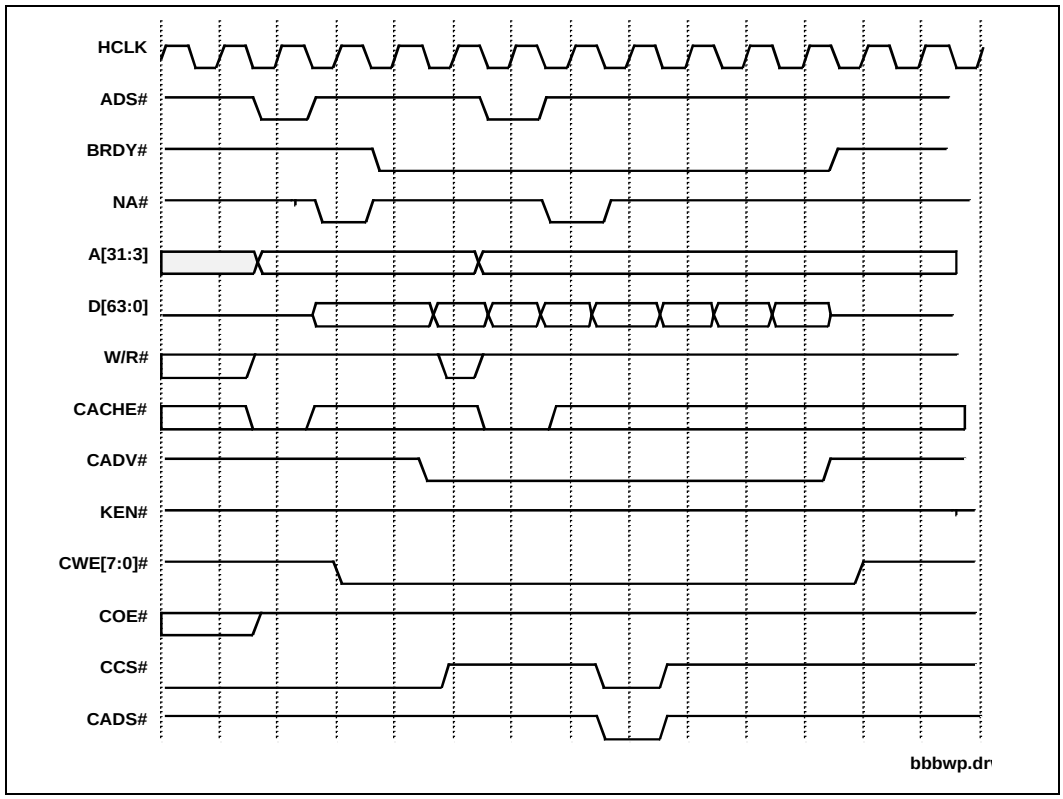
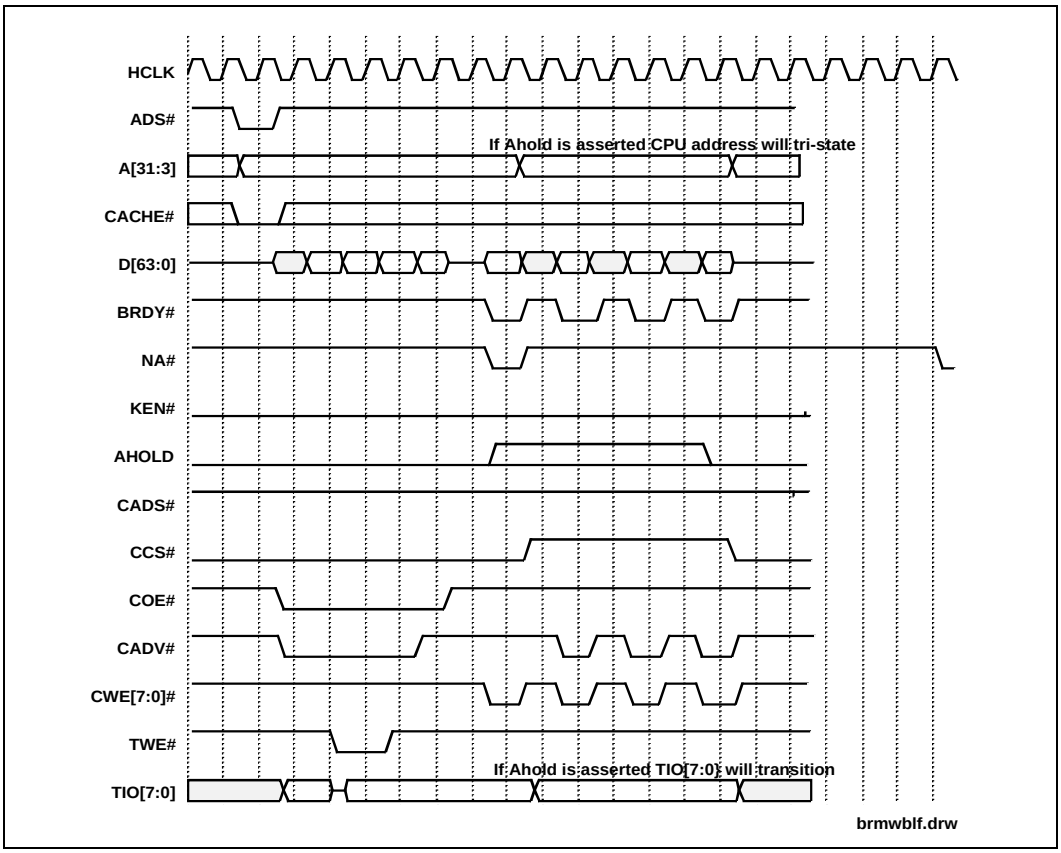


Figure 17. L2 Cache Read Miss, Write-Back, Line Fill, Pipelined Burst SRAM



2.2 DRAM Timing Relationships

Figure 18. Burst Read Page Hit (EDO)

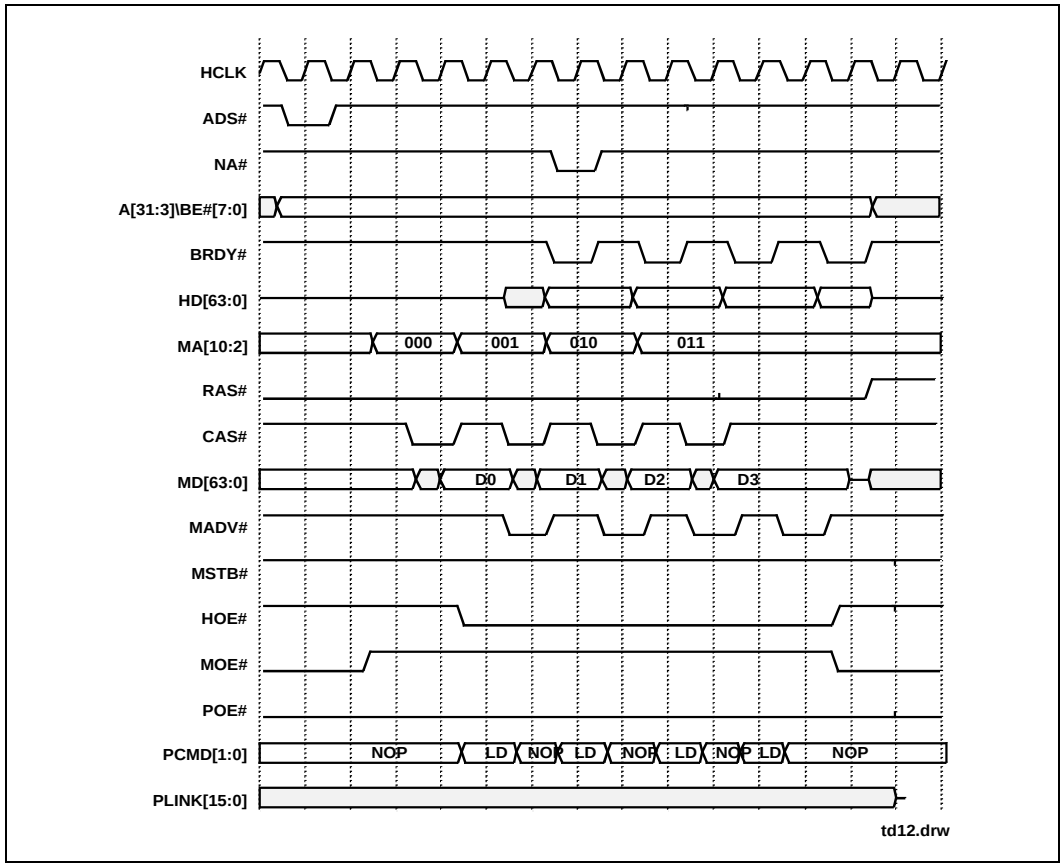


Figure 19. Burst Read Row Miss (EDO)

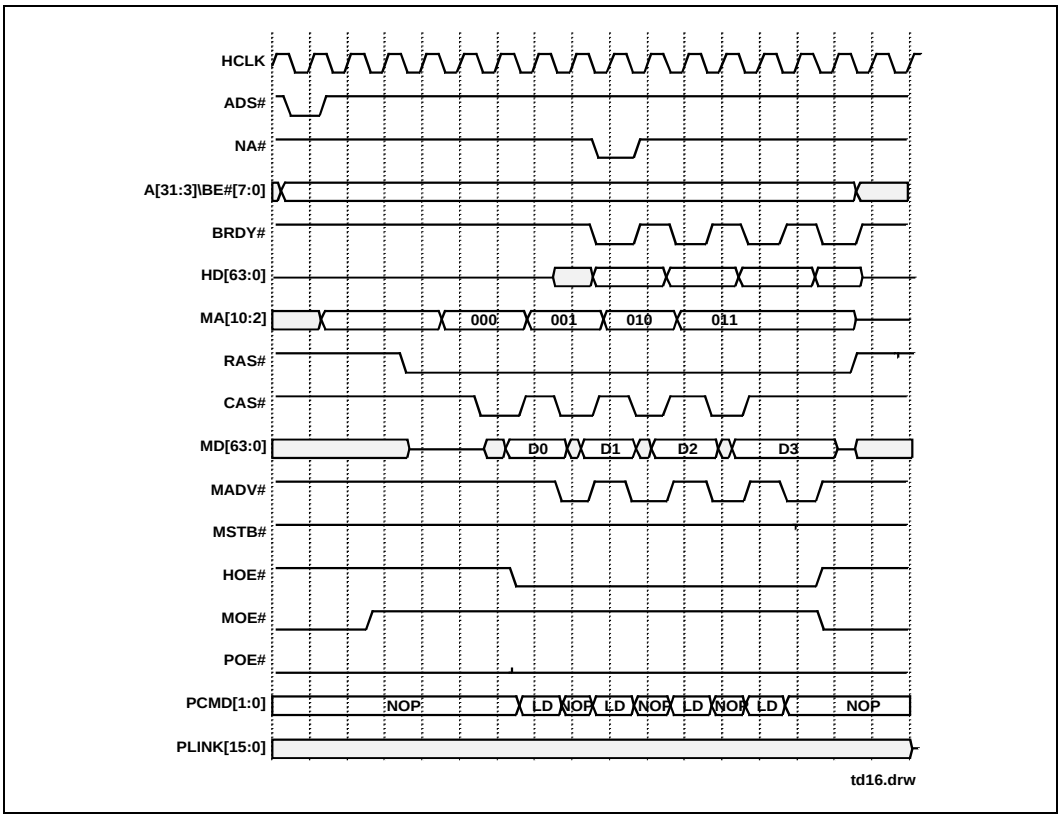


Figure 20. Burst Read Page Miss (EDO)

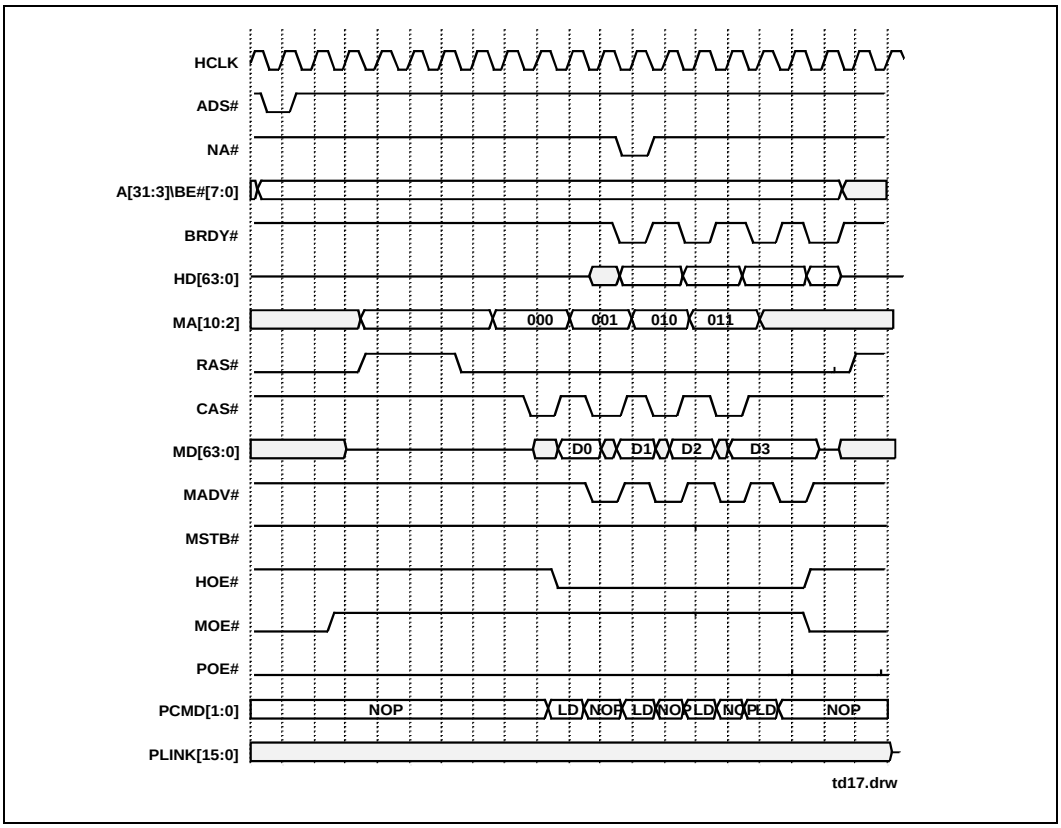


Figure 21. Burst Read Page Hit (Standard Page Mode)

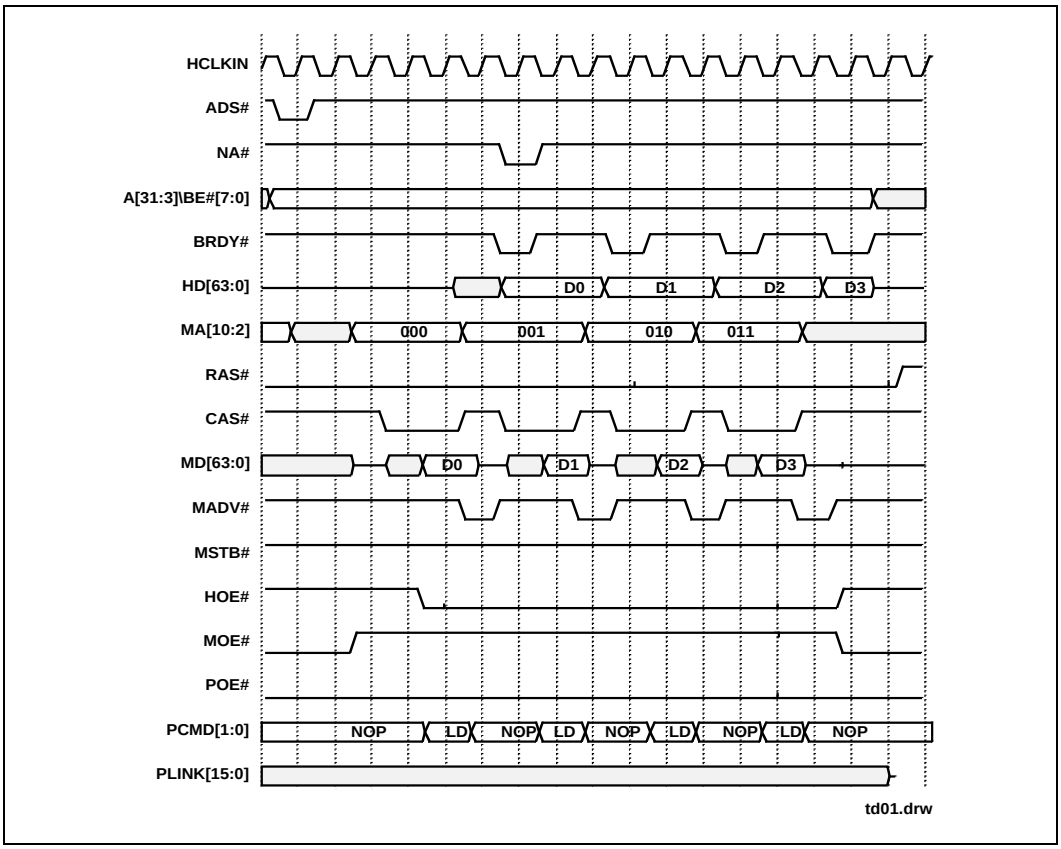


Figure 22. Burst Read Row Miss (Standard Page Mode)

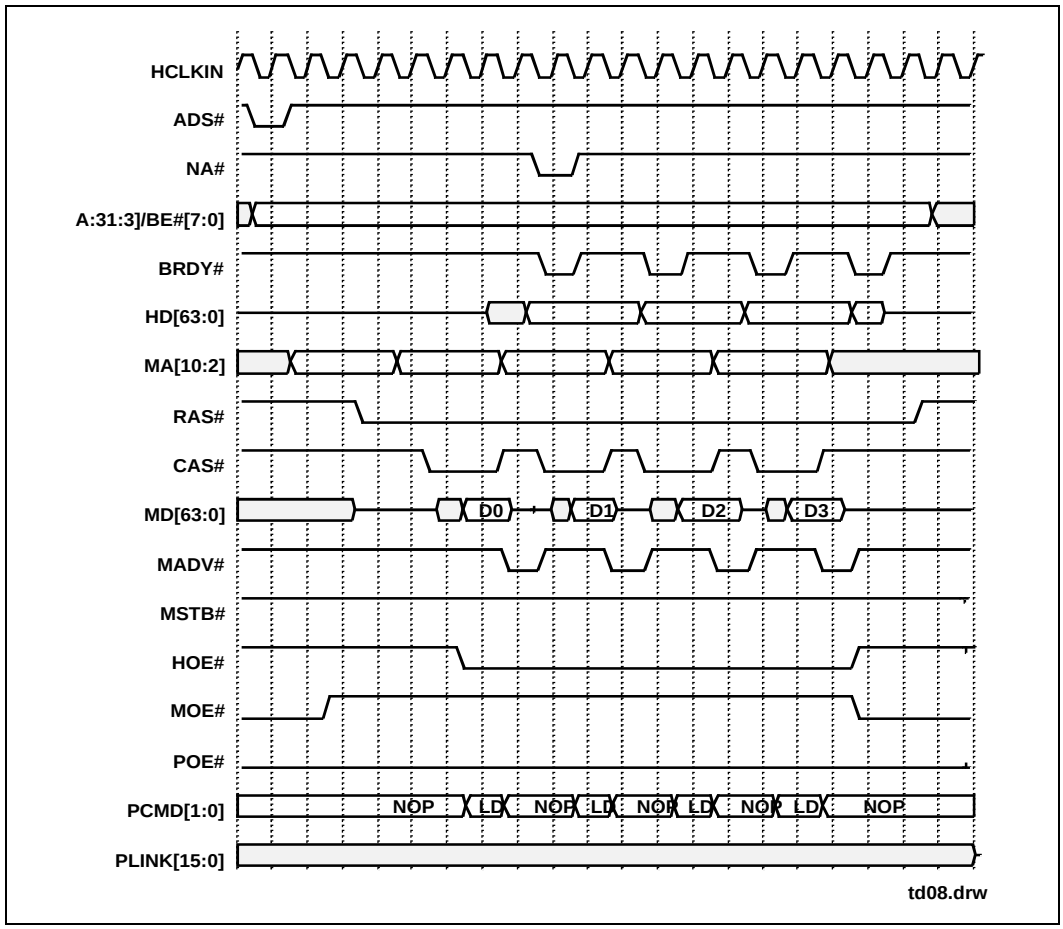


Figure 23. Burst Read Page Miss (Standard Page Mode)

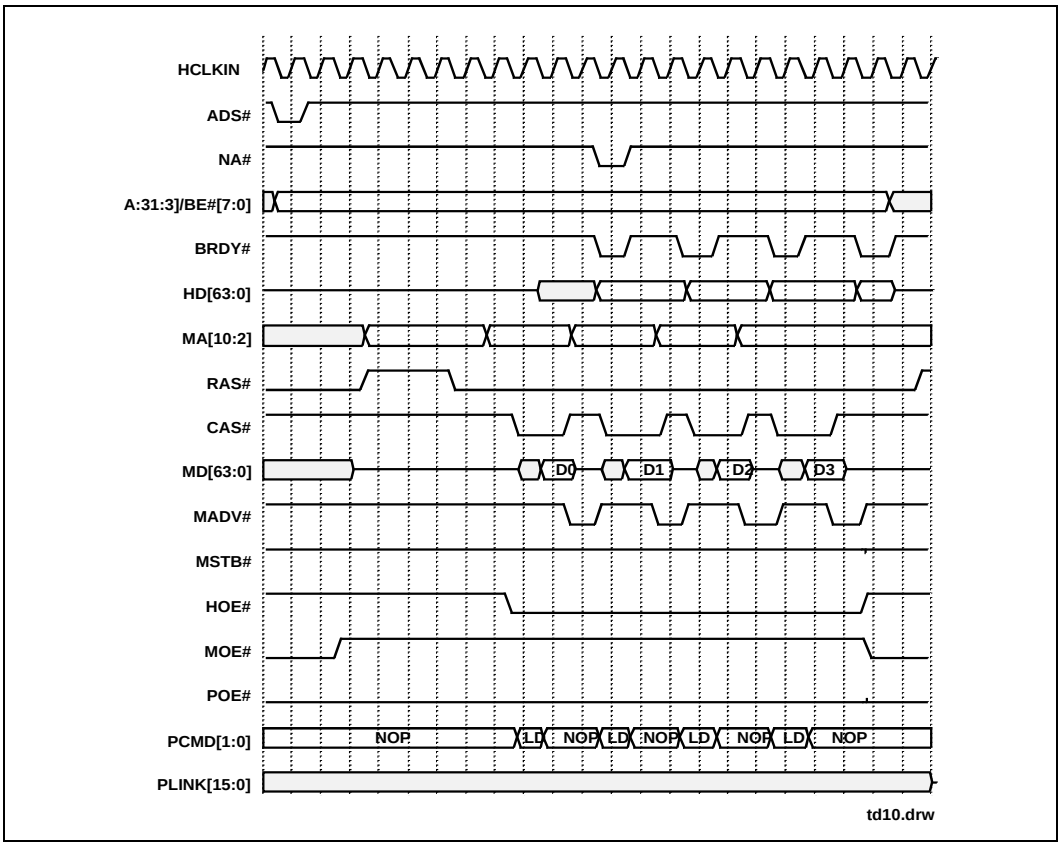


Figure 24. Posted Burst Write Page Hit

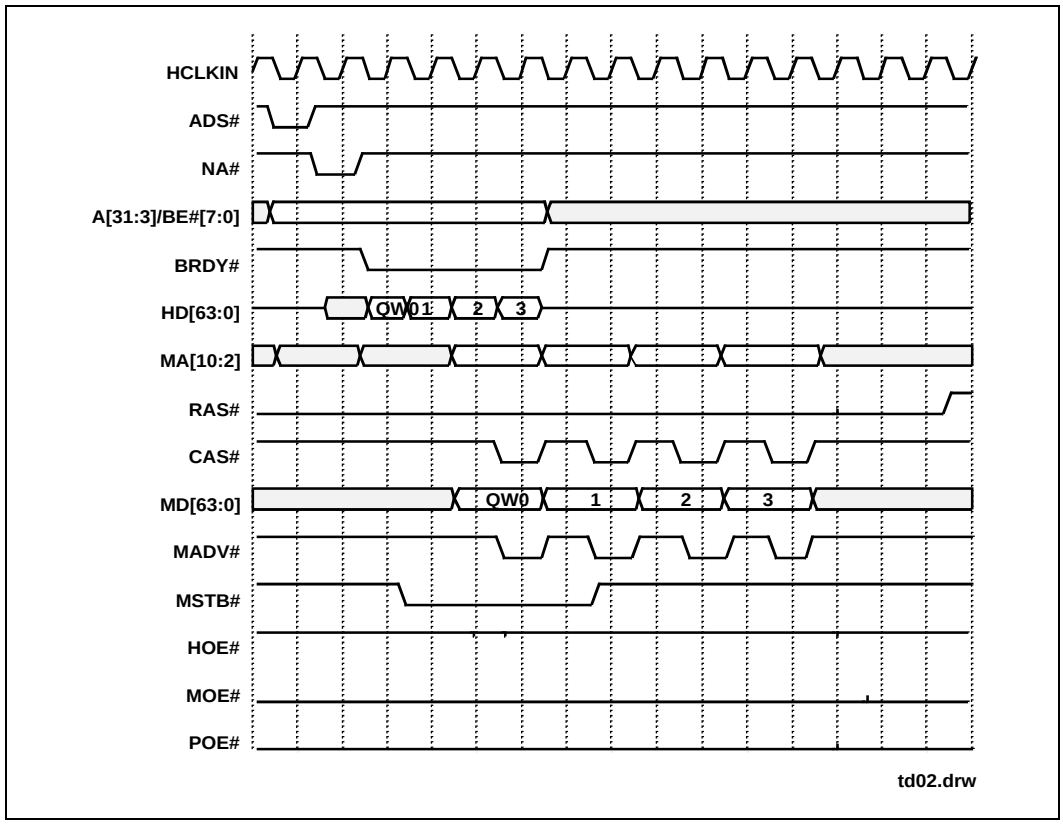


Figure 25. Burst Write Row Miss

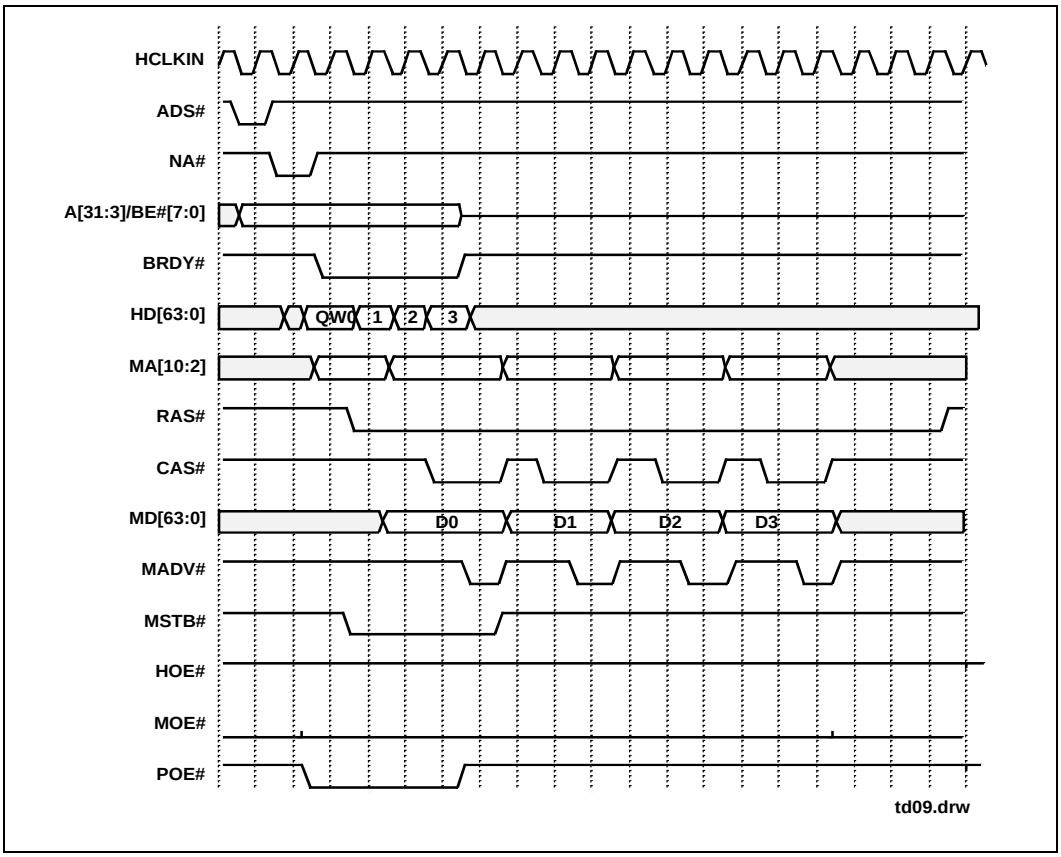


Figure 26. Burst Write Page Miss

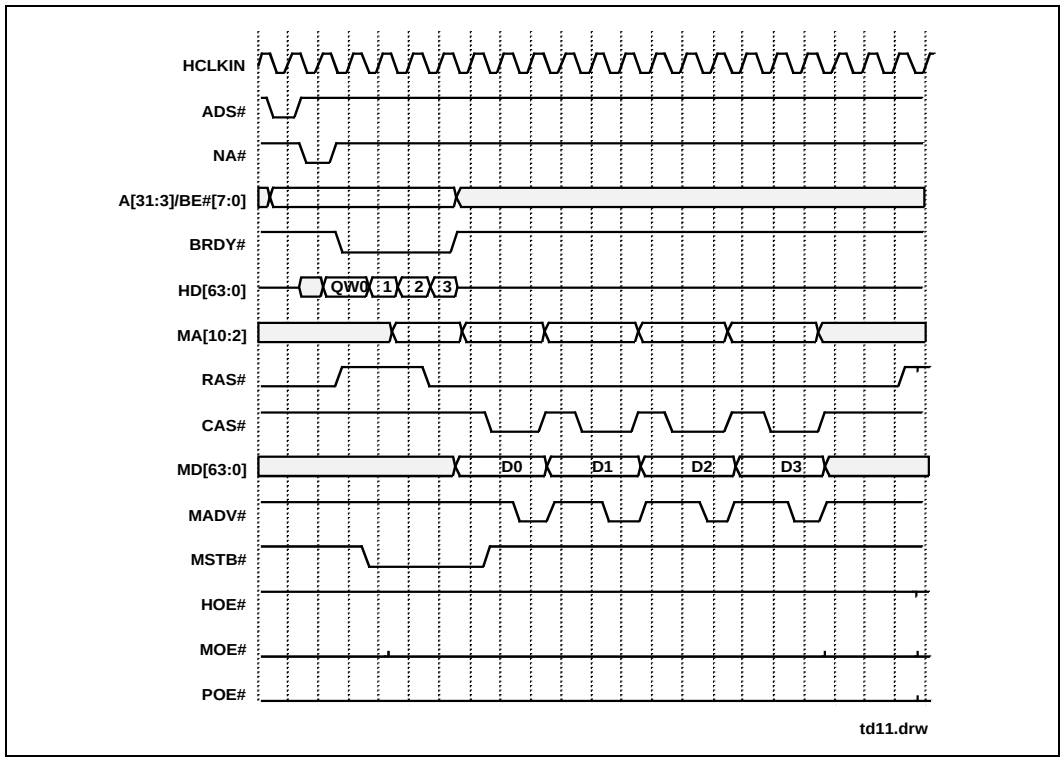
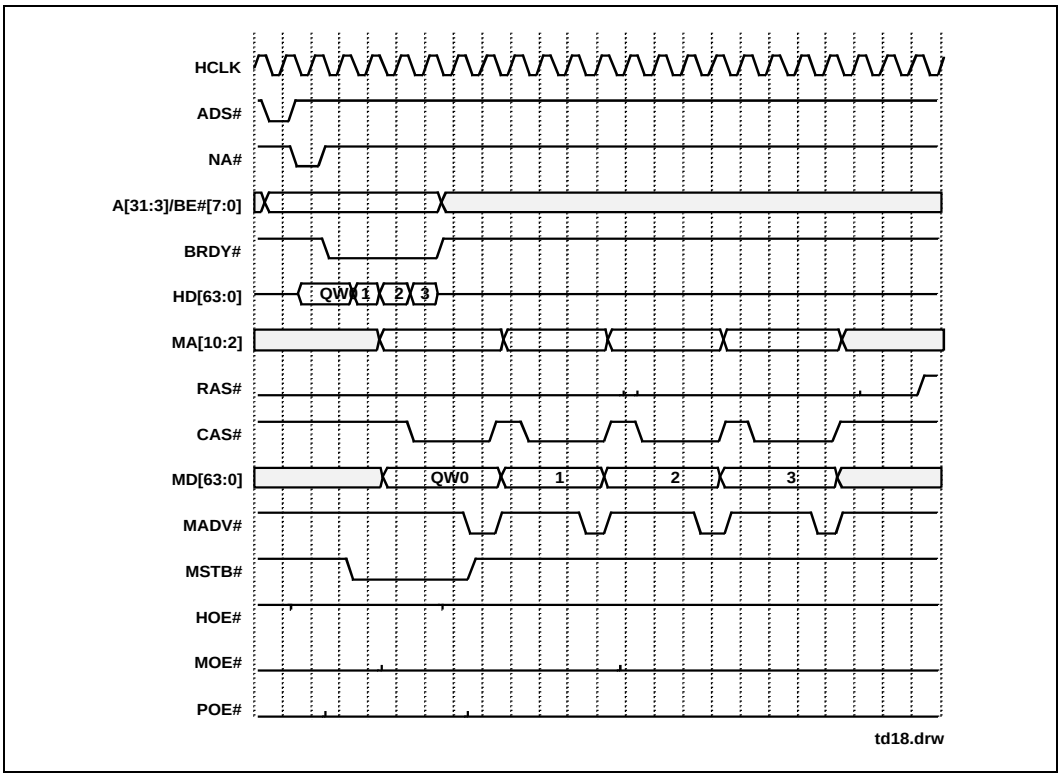


Figure 27. Burst Write



2.3 Additional Timing Relationships

Figure 28. CPU to PCI Write Cycle

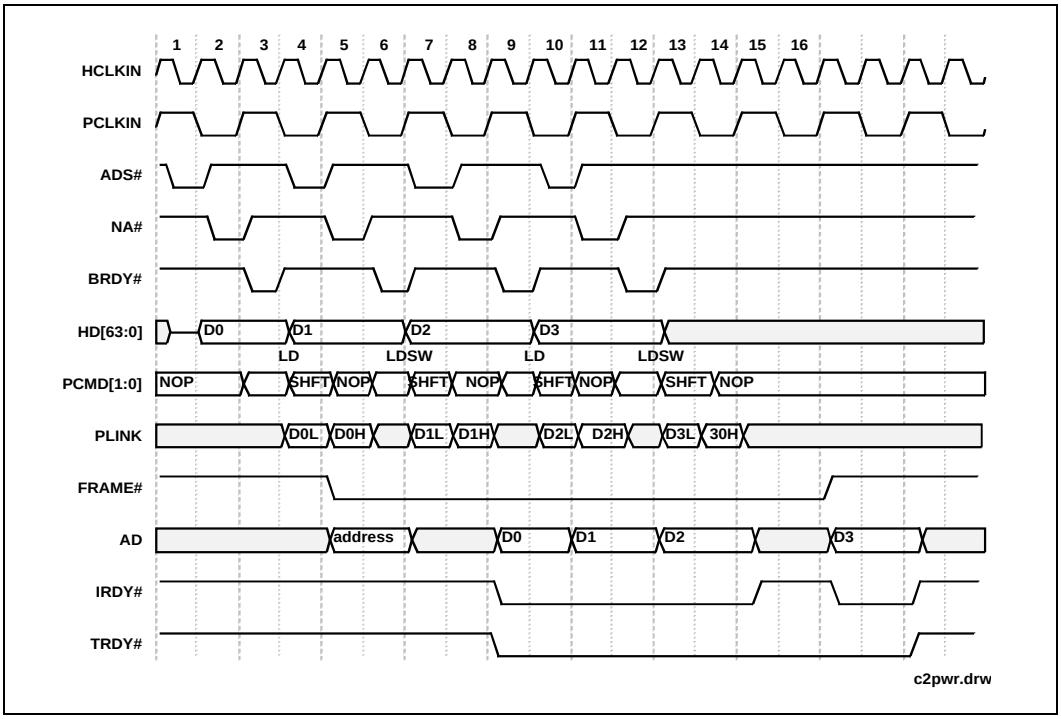


Figure 29. CPU to PCI Memory Read Cycle

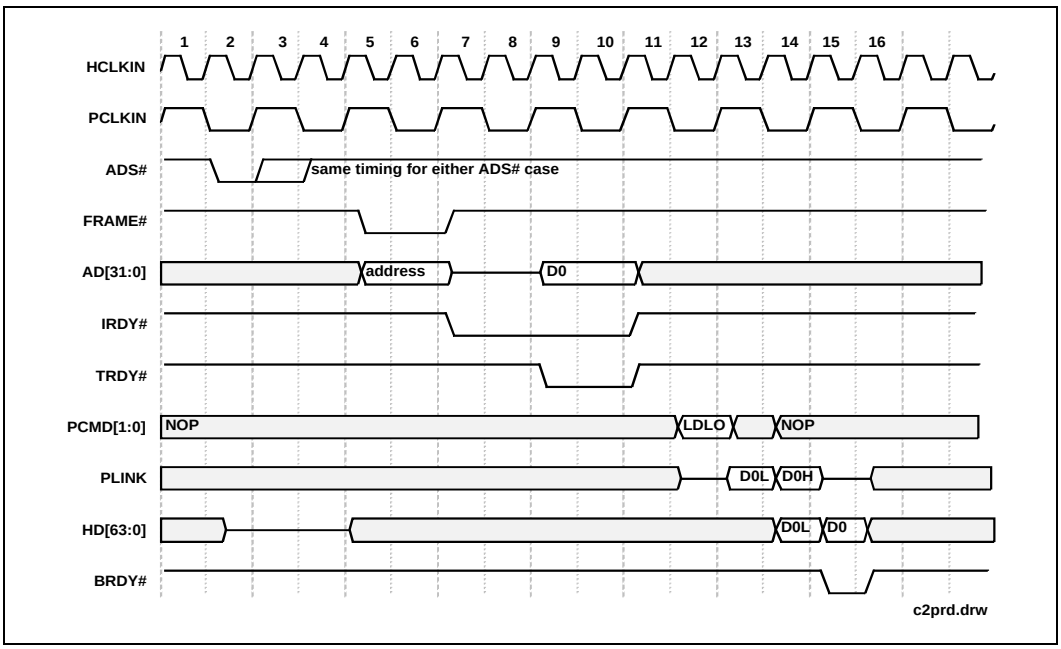


Figure 30. PCI Bus Master to DRAM Write Cycle

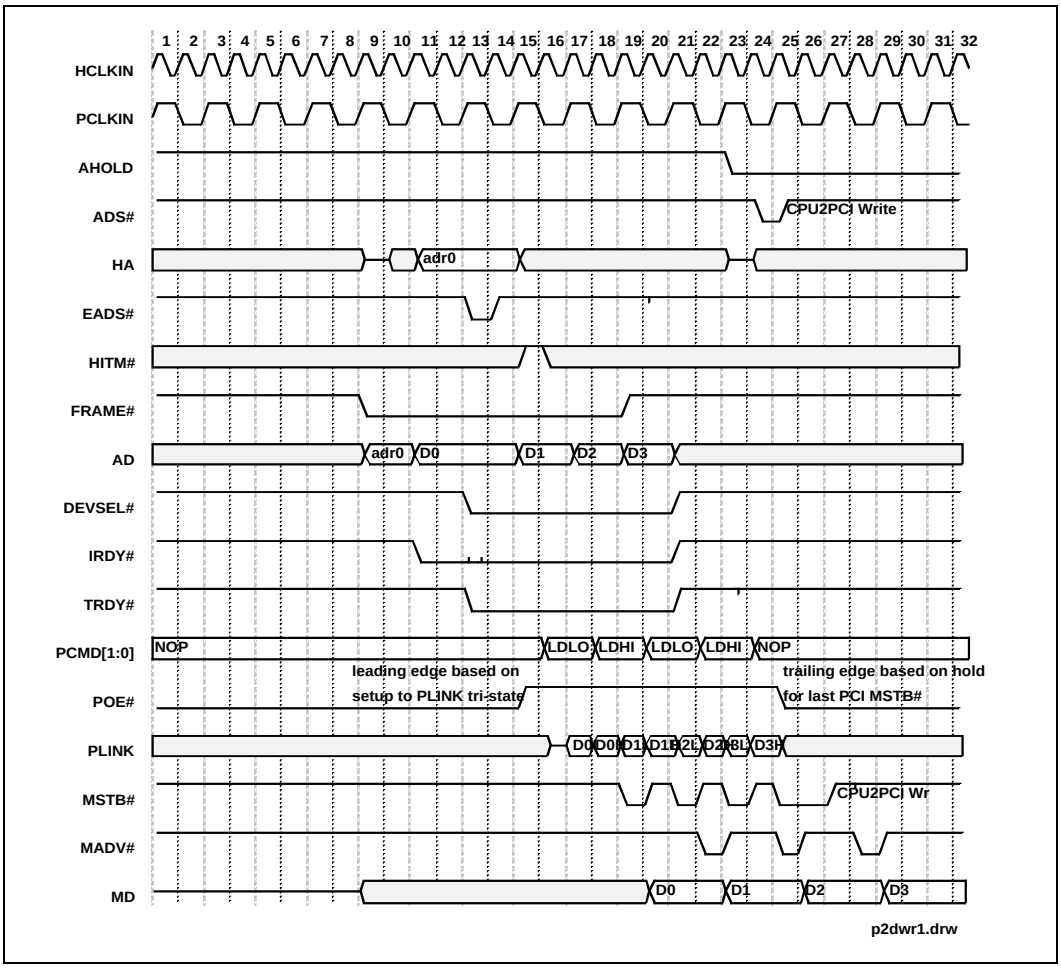


Figure 31. PCI Bus Master Read From DRAM

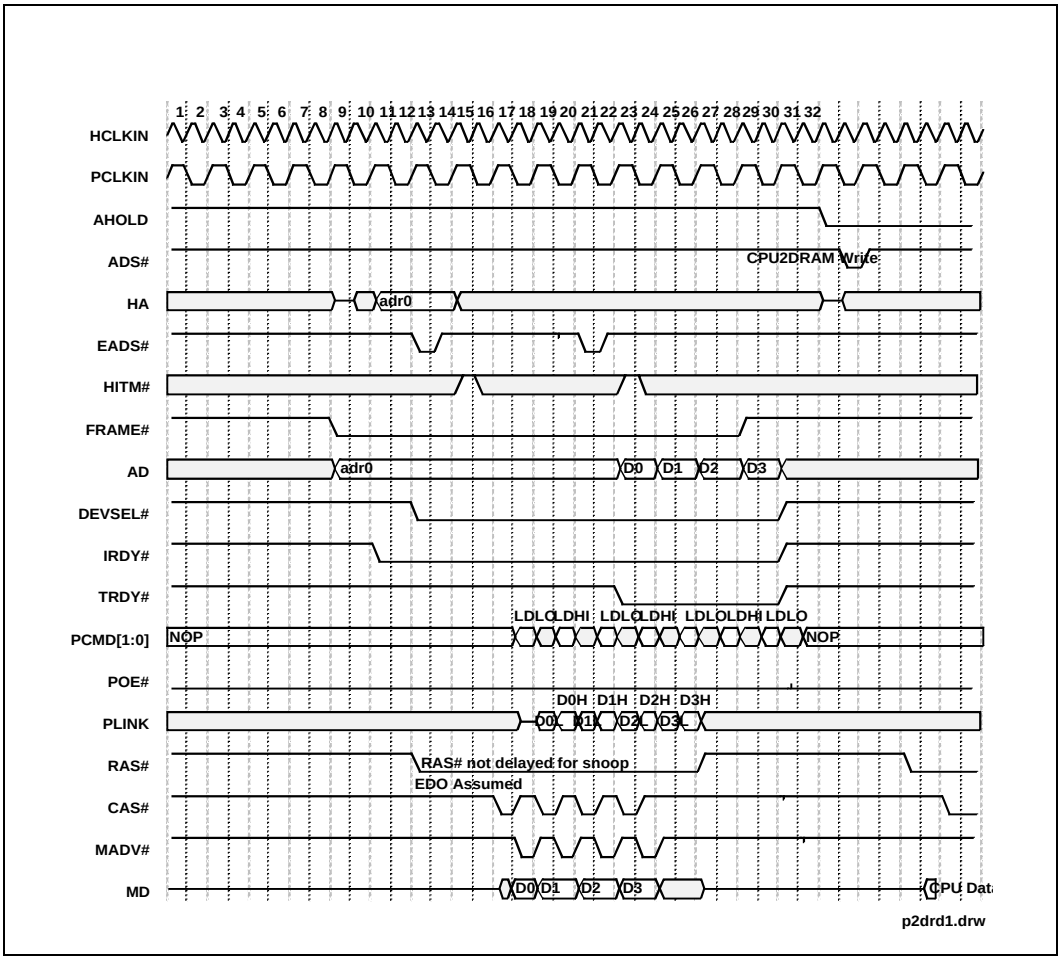


Figure 32. RAS Only DRAM Refresh Cycle